Modeling SiO_2 Ion Impurities Aging in Insulated Gate Power Devices Under Temperature and Voltage Stress

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ABSTRACT

This paper presents a formal computational methodology to explain how the oxide in semiconductors degrades over time and the dependence of oxide degradation on voltage and temperature stresses. The effects of aging are modeled and quantified by modification of the gate-source capacitance value. The model output is validated using experimental results of a thermally aged power semiconductor device.*

1. INTRODUCTION

Device aging produces shifts in threshold voltage (Vth) and capacitance parameters, primarily due to mobility of impurities, especially Na^+ Ion (Kerr et al., 1964). This phenomenon was an important reliability issue in the early stages of MOSFET fabrication because of the primitive fabrication process. As the manufacturing technology evolved and more pure silicon dioxide material could be grown on devices, less importance was placed on ion migration loss in reliability research (Miranda and Sune, 2004; Feinberg et al., 2000; Feinberg and Widom, 2000). For power devices that are fabricated with vertical technology, oxide contamination and field distortion are the predominant failures (Clemente and Teasdale, 1993). Semiconductor reliability, especially for power devices has improved markedly in the last decades but at the same time interest in life assessment for end of life predictions with associated confidence levels has emerged as a very important area. This created a new space that merges the lessons learned from traditional reliability with early diagnosis and prognosis. We explore that space in this work by using ion mobility as an aging indicator in insulated gate power devices, such as IGBTs and Power metal oxide semiconductor field effect transistors (MOSFETs).

2. POWER SEMICONDUCTOR STRUCTURE

The main silicon power devices are power MOSFETs and IGBTs; the first are used mainly in applications with less than 200 Volts while IGBTs are the preferred option for greater voltages. The power device structures are different from the highly integrated low power devices because they use different manufacturing processes and technologies. In order to support high electric fields associated with the power, the preferred choice is vertical device construction with a large integration of dispositive in parallel. The geometric disposition connecting individual devices in shunt create well-known devices such as the HexFET™ (Clemente et al).

2.1 Power MOSFET Structure

A general structure of a vertical power MOSFET device is shown in Figure 1. A power device is constructed by creating a mesh of vertical devices positioned in parallel to create high power. Therefore,

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14. ABSTRACT
This paper presents a formal computational methodology to explain how the oxide in semiconductors degrades over time and the dependence of oxide degradation on voltage and temperature stresses. The effects of aging are modeled and quantified by modification of the gate-source capacitance value. The model output is validated using experimental results of a thermally aged power semiconductor device.

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the structure shown in Figure 1 is connected in parallel to be combined into a power MOSFET.

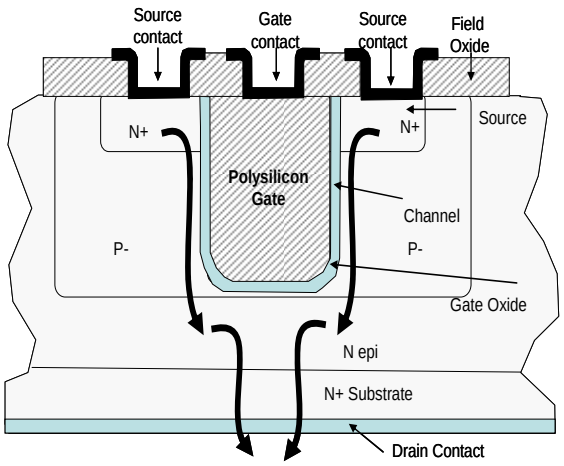

Figure 1: Structure of a commercial vertical power MOSFET

Parasitic components define the properties and behavior of a semiconductor power device. These properties change over time, providing important tools for early precursors to failures. Figure 2 shows a diagram with the material that creates the oxide and the disposition of the main three parasitic capacitors that are characteristic of a power semiconductor: Cgs (gate-to-source), Cds (drain-to-source), and Cgd (gate-to-drain).

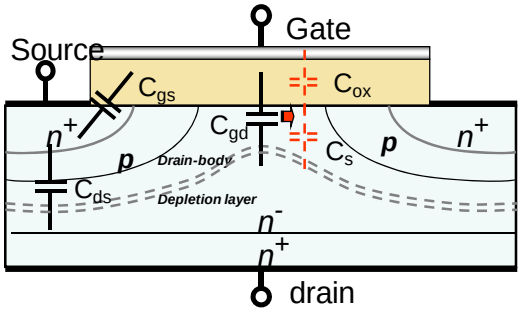

Figure 2: Parasitic component of a vertical power MOSFET

2.2 IGBT Structure

The parasitic structure of the IGBT is similar but more complex than the vertical MOSFET shown in the previous section. Due to the similarity of the internal parasitic structure, this paper performed the experimental result on the IGBT, as the results should be similar. Figure 3 shows a detail of the parasitic structure and the circuit representation of the IGBT.

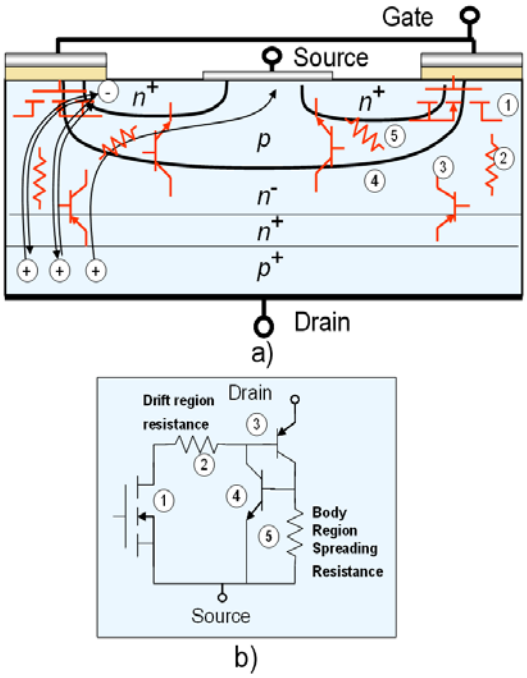

Figure 3: IGBT parasitic structure and circuit representation

Figure 4 shows the two components (fast diode and N-Type IGBT) integrated into the power device and encapsulated in the TO-220AB package corresponding to the IGBT IRG4BC30KD from International Rectifier. It also shows the X ray image of the IGBT with a freewheeling diode as part of the device package.

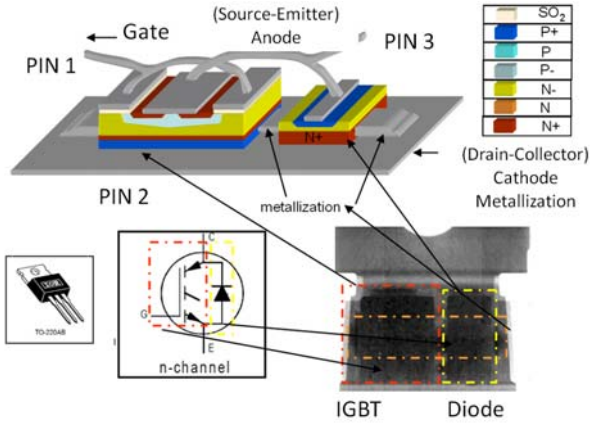

Figure 4: Structure of a commercial vertical power IGBT

2.3 Power Device Stress Factors

Industry reliability practices have led to classification of vertical power devices stress and failure factors in two distinct categories: silicon die defects and die

packaging defects (Scroder, 1990; Clemente et al., 1993; Crook, 1979). The die defects in MOSFETs are generally categorized under field distortion defects and oxide defects. Field distortion defects are a result of the electric field in the MOSFET getting distorted. This distortion is caused when a high voltage is applied to the device in presence of polar molecules. A polar molecule is such that one end of the molecule is positively charged and the other end is negatively charged (e.g., water and atmospheric ionic contaminants). Oxide defects are the second most common failures associated with die defects. Defects in the MOSFET's layer of gate oxide can cause failures such as short-circuiting from gate to source. These defects are often caused by thermal damage due to thermal cycling, which in turn leads to more trap generation. These traps cause more conduction and eventually the short-circuiting.

The die packaging defects fall under several categories: die attach damage, wire bond fatigue, and metal corrosion. Die attach defects are caused by thermal differentials created between the die and the headers of the MOSFET devices. The ultimate result is creation of voids and cracks in the die attach region leading to degradation in the on resistance and thermal resistance of the device. Wire bond fatigue is also thermally induced and results in the separation of the wire bond of the MOSFET device. Finally, metal corrosion occurs due to intrusion of water particles into the device packaging through the atmosphere.

Naturally, introduction of water in the metallic contact area leads to corrosion and that eventually results in device degradation in the form of on-state resistance shift.

3. SWITCHING PROCESS

Figure 5 shows how the different parasitic capacitances influence the switching turn-on process (Mohan, et. al). The subfigures (a) through (d) show the equivalent circuit for the MOSFET to estimate the characteristic voltage and current in the device as the switching process progresses. Figure 5 (a) and (b) show how the power transistor begins to switch with the current initially circulating by the freewheeling diode DF. During these stages, the influence of Cgd (gate-to-drain) and Cd (drain-to-source) with R_G, the gate resistance, is very important. In the final stages shown as (c) and (d) R_{DS}, drain-to-source resistance, together with Cgd defines the process.

Figure 6 summarizes the influences of the capacitances in the switching time during on-state and how the variation in the values of the parasitic parameters will affect the time spent in the different stages. The gate drive voltage signal is a step response whereas the other gate to source voltage (VGS) and gate and drain currents are show. It should be noted that subfigures (a) through (d) in Figure 5 are correlated with stages 1 through 4 in Figure 6. These figures show the effect of parasitic capacitance on the characaristic waveforms of the device.

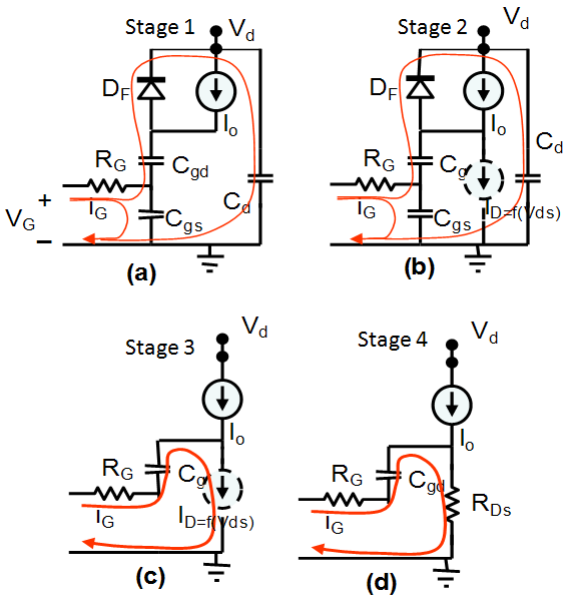

Figure 5: Capacitance interaction during switch-on

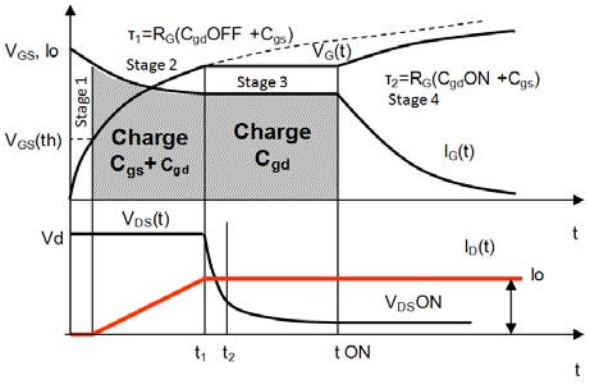

Figure 6: Effects of parasitic capacitance as a function of time

Given the influences of internal parasitic elements of power semiconductors, it is then important to classify the effects of aging in these parasitic elements. Figure 7 shows a schematic of how aging can be represented in changes of parasitic capacitance over time. Figure 7 shows the model of the power MOSFET with the relevant parasitic elements during switch on process. The (a) thorugh (d) subfigures show the model simplification by lumping the components together. Increasing the power losses during switching can be

represented as regular increases of the value of R_G. Moreover, the changes in the capacitance by ion movement or new trap charges can be accounted for as changes in C_G over time. Section 7 provides more details as to how this process occurs. Figure 7(d) is the model this paper considered for evaluation, specifically the Cg is the parastic element that modeled and monitored in the aged power device to characterize the aging effects. Other works (Celaya et.al, 2009) have used on-resistance $R_{DS\ on}$ as an indicator of device aging.

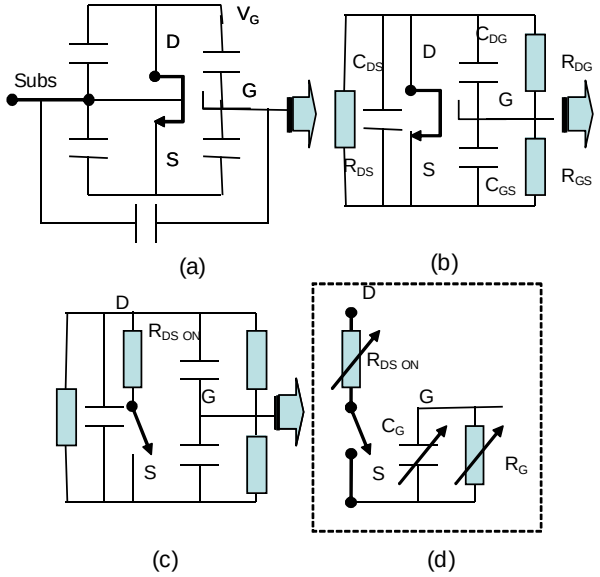

Figure 7: Power device simplified circuit aging

4. POWER DEVICE RELIABILITY

The previous section highlights some of the common and widely accepted reliability issues presented with the design and operation of MOSFET/IGBT power devices. In this section, traditional semiconductor reliability concepts are related to remaining life estimation.

From a reliability engineering point of view, the failure rates caused by factors described in the previous section have to be addressed and taken into consideration.

The mean time to failure (MTTF) is usually defined by the inverse of the failure rate of devices:

$$MTTF = \frac{1}{\lambda} \quad (1)$$

where λ is the failure rate.

A failure rate (λ) could be estimated by

$$\lambda \propto \frac{1}{TDH * AF} \quad (2)$$

Where:
AF: Acceleration factor
TDH: Total duration hours

Semiconductor manufacturers perform millions of hours of testing to determine failure rates. This gives extremely valuable information for the reliability of their product. Additionally, applying this concept with more emphasis on the acceleration factor yields important information for life estimation.

The AF is generally determined from the Arrhenius equation but can also be determined using a power law, as is common industry practice.

4.1 Field Distortion Acceleration Model

Acceleration models for the reduction of life in equipment have been used extensively. Representative examples include the Arrhenius model for temperature (Leblebici and Kang, 1993):

$$L(T) = AF \cdot e^{\frac{E}{kT}} \quad (3)$$

The acceleration factor, AF, is determined generally from the Arrhenius model:

$$AF = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \quad (4)$$

D.L Crook (Crook, 1979) proposed the following expression in the case of two acceleration factors (temperature and voltage):

$$AF = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \cdot \exp\left(-\frac{E_2 - E_1}{E_c}\right) \quad (5)$$

where:

Ec has been experimentally (Crook) been shown to equal 0.062 MV/cm.

Equation 6 shows the Power Law that is used commonly in determining the life expectancy of power devices based on the data presented in (Pearce et al.) Several manufacturers use gate voltages and temperatures for aging estimation. Based on the data (Pearce et al.) the values for the IRF4XX series are computed to be A=-17.2, B=0.4, C=-0.15 and the respective curves are shown in Figure 8.

$$AF = A * 10^{CT} * 10^{B*V_G + a} \quad (6)$$

The thermal activation energy of a failure mechanism is determined by testing at a minimum of two different temperature stress levels as is shown in Figure 8. Figure 8 shows the power MOSFET life expectancy using Power Law shown in equation 6. It can be seen that the life expectancy of MOSFET

devices changes with the varying bias voltages and are uniformly changing as the operating temperature changes. In lab testing and field operations, it has been shown that device's failure gets accelerated when operated in higher temperature regions.

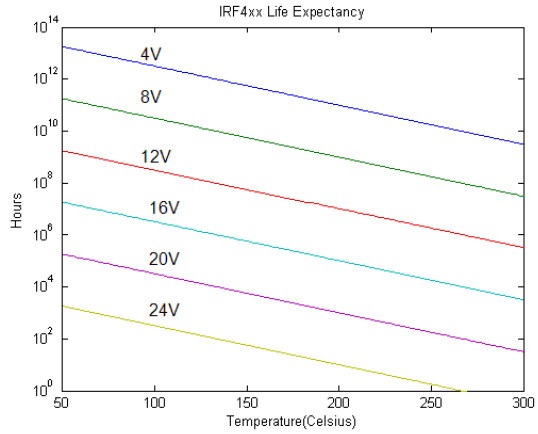

Figure 8: Power MOSFET life expectancy under Power Law

Figure 9 illustrates the concept of using a hybrid acceleration life expectancy modeling. The hybrid model concept combines the Power Law and Arrhenius models. Doing so allows for a more realistic representation of life expectancy of power MOSFET devices based on extensive reliability studies and operational usage. The two stress factors, temperature and bias voltage, take predominant effects in different regions based on the level of temperature stress. At low temperatures, the bias voltage remains the dominant factor; however, at high temperature a new phenomenon rules the process. At higher temperatures, the life expectancy goes down much faster in accordance with the Arrhenius model. Moreover, the variation in the gate voltages does not remain a factor in the life expectancy for all but the 24 V bias voltages as shown in Figure 9.

5. THERMAL AGING

The devices under test for this study are the same devices used for the identification of precursors of IBGT failure presented in (Celaya et al., 2009). Several IGBTs were aged under thermal overstress in order to accelerate the life of the components through latch-up failure or thermal runaway. The thermal overstress was generated by power cycling the devices, resulting in a controlled thermal cycling. As stated in (Patil et al., 2009), it was observed that for aged devices, there is an increase in threshold voltage and C-V tests were used to identify the failure mechanism. In addition, die attach degradation was observed in CSAM images of the aged devices resulting in a drop of collector-emitter ON voltage.

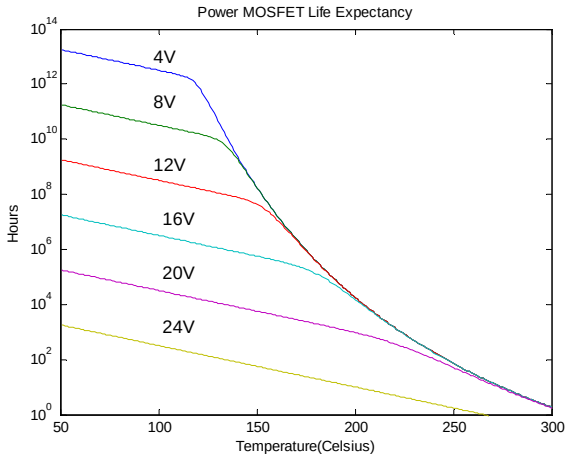

Figure 9: Power MOSFET life expectancy under the hybrid model

The devices under test are discrete IGBTs from International Rectifier (IRG4BC30KD). These devices are rated at 600V collector-emitter voltage, 15A collector current and are in a TO-220 package.

5.1 Accelerated Aging System

In order to evaluate the aging effects in power semiconductors, accelerated aging systems have been used to quickly induce aging effects in devices while keeping them operational. The aging system used for this experiment is described in detail in (Saha et al., 2009). The system allows for accelerated aging of gate controlled power transistors like power MOSFETs and IGBTs. Custom-made software controls the accelerated life experiments and logs data for further analysis. A high level block diagram is presented in Figure 10; details on the hardware and software implementations are available in (Sonnenfeld et al., 2008).

In terms of accelerated life testing, the system can apply different stresses like thermal, electrical or a combination of them. The focus here is on thermal cycling which is achieved by doing power cycling on the devices under test. The system allows the investigation of different failure mechanisms (intrinsic and extrinsic) like dielectric breakdown, hot-carrier injection, electro-migration, contact migration, wire lift, die-attach degradation and package delamination. This aging system was designed based on the work presented in (Ginart et al., 2007) and it has been used in the aging of IGBTs and power MOSFETs in order to understand failure mechanisms, identify precursors of failure, and develop degradation models for prognostics and health management of these devices (Celaya et al., 2009; Patil et al., 2009; Saha et al., 2009; Sonnenfeld et al., 2008).

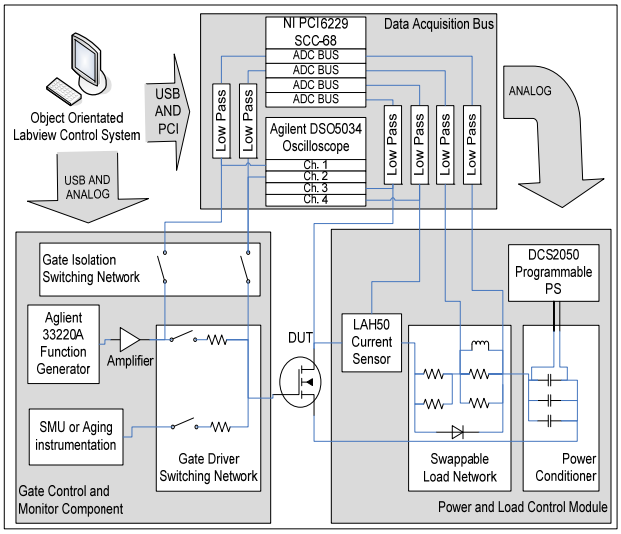

Figure 10: High-level diagram of accelerated aging system

5.2 Aging experiments

The accelerated aging applied to the devices presented in this work consists of thermal cycling to accelerate degradation using thermal overstress. The failure condition was considered as latch-up or thermal runaway. Thermal cycles were induced by power cycling the devices without the use of external heat sink. This reduced the heat dissipation capabilities of the devices, allowing the self-heating of the device due to the power switching operation. The IGBT package temperature was the controlled variable for the thermal cycling. The temperature was measured in situ using an infrared sensor. For the aging power cycle, the gate voltage was a square signal with amplitude of 8V, a frequency of 1 KHz and a duty cycle of 40%. Proper amplification of the signal ensured that enough current is available to charge the gate of the IGBT at the selected frequency and duty cycle. The collector-emitter was biased at 4V and a resistive load on the order of 0.5 ohms was used on the collector side of the device.

The temperatures are controlled within low and high temperature bounds. The device was set on the power cycling regime if the case temperature was below the lower threshold and it was turned completely off if the temperature reached the upper threshold. This hysteresis controller provided the thermal cycles needed to accelerate the age of the device. It should be noted that currents and voltages were maintained within the safe operating area while the temperature was raised beyond the maximum rating to induce latch-up. The high temperature bound was set to 300°C, resulting in failed IGBTs due to loss of gate control or thermal runaway. The aging time (time to failure) under these aging conditions ranged from 30 minutes to 2 hours. Additional details are documented in (Celaya et al., 2009).

6. SIMULATION & RESULTS

6.1 Aging Stress Factor and Capacitance Shift

The capacitance mainly changes by mobility of trap charges during fabrication and additional traps generated during operation as shown in Figure 11. These charges are created mainly from bias voltages and temperature. Regardless of the origins of the impurities, the mobility of impurities produces a variation of capacitances that can be used as an indicator of aging in the semiconductor devices. Aging in semiconductors usually has multiple failure mechanisms that develop simultaneously before the predominant mechanism becomes evident and finally leads to device failure. In vertical device structures the main failure mechanisms that have been reported are: void formation from the packaging side and from the device itself (Saha et al., 2009; Sonnenfeld et al., 2008; Ginart et al., 2007; Srinivasan, 2000), oxide damage and field distortion (Pearce et al., 1993). Void formation leads to increase of the junction temperature which in turn leads to failures. The oxide damage and field distortion mechanisms are the main focus of this work. For both failure mechanisms the capacitance changes with the realignment of the trap impurities, showing the aging progression in the $Si0_2$.

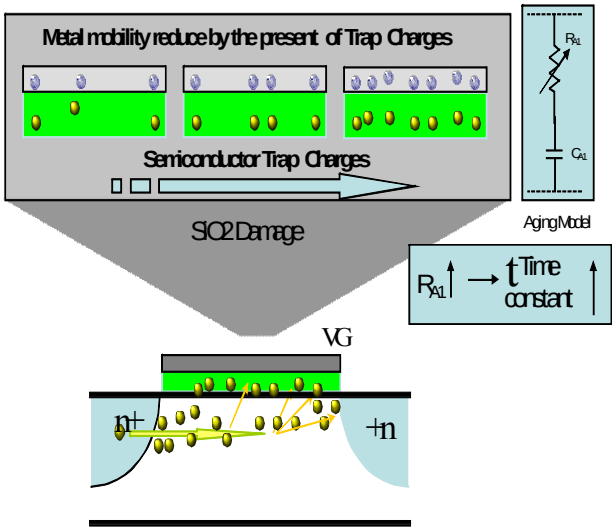

Figure 11: Metal mobility reduced by the presence of trap charges

The IGBT parameters for the device used in for evaluation in this paper are shown in Table 1. The

IGBT device used in this paper is IRG4BC30KD from International Rectifier.

Table 1: IRG4BC30KD relevant parameters

IGBT				
Internal Emitter Inductance (L_E)	7.5nH			
Output Capacitance (C_{oes})	110 pF	C_{GE}= 900 pF C_{CE}=83 pF C_{GC}=27pF	V_{GE}=0 V_{CC}=30V f=1Mhz See Figure	
Input Capacitance (C_{ies})	920 pF			
Reverse Transfer Capacitance (C_{res})	27 pF			
DIODE				
Reverse recovery time	42ns	60ns (max)	I_F=25°C	I_F=12A V_R=200V di/dt=200µA
	80ns	120ns (max)	I_F=125°C	

6.2 Fundamental equations and modeling

In this work, only the initial trap charge is included in the model whereas the trap generation process will be included in the continuing future work. The equations that govern the potential changes in the oxide semiconductor interface are shown below (Pierret, 1996):

$$\Delta\phi_{ox} = \frac{K_s}{K_o} x_o \varepsilon_S - \frac{1}{K_o \varepsilon_S} \int_o^{x_0} x \rho_{ox}(x) dx \qquad (7)$$

where:
K_s is the semiconductor dielectric constant
K_o is the oxide dielectric constant,
x_o is the oxide thickness,
ε_s is the electric field in the semiconductor at the oxide-semiconductor interface,
ρ_{ox} is the charge density in the oxide.

This implies that for the same Φ_S:

$$\Delta V_G = -\frac{1}{K_o \varepsilon_S} \int_o^{x_0} x \rho_{ox}(x) dx \qquad (8)$$

Finally, computing the capacitance for a nonideal MOSFET/IGBT

$$C = \frac{C_o}{1 + \frac{K_o W_t}{K_s x_o}} \qquad (9)$$

where W_t is the depletion width calculated by

$$W_t = \left[\frac{2 K_S \varepsilon_o}{q N_A} (\phi_{ox}) \right]^{1/2} \qquad (10)$$

where ϕ_{ox} is the oxide potential related to the semiconductor doping concentration, and Co is the oxide capacitance computed by

$$C_o = \frac{K_o \varepsilon_0 A_G}{x_o} \qquad (11)$$

where A_G is the gate area.

Following the Arrhenius equation shown in Equation 5, the diffusion-like movement of trap charge impurities caused by stress induced aging is modeled as time moves forward. The diffusion process mobilizes the impurities in an exponential fashion as a function of temperature and the bias voltage, V_G, thus changing the oxide potential as defined in Equation 7. Therefore, the change in the oxide potential leads to the depletion width changing ultimately produces the shift in the device capacitance with respect to the voltage.

Figure 12, Figure 13, and Figure 14 show the MATLAB simulation results of the mobility of the trap charge impurities in the power devices and the corresponding shift in the capacitance. The simulation results are shown for the time scale of one, ten, and thirty years. The temperature was kept constant at 100°C along with the initial trap charges and the gate voltage V_G was set at 8V. The impurities, represented per m^2, are shown to migrate over time from being uniformly distributed across the device (year 1) and aggregating on one end by year 30. Correspondingly, the capacitance starts varying and the shift over time is shown. The initial capacitance is shown in blue circles whereas the simulated capacitance at the respective time is shown in a red line, illustrating a clear shift in capacitance over time as migration of impurities starts accelerating.

6.3 Experimental Results

An experiment to validate the simulation results was conducted on an IGBT, which has a similar gate structure as that of a MOSFET. The IGBT was subjected to the stress profiled in Figure 15. The stress estimated was equivalent to a reduction of the remaining useful life (RUL) of the IGBT device. This estimation in the RUL is based on the life expectancy law modeled for high temperature stress as shown in Figure 9.

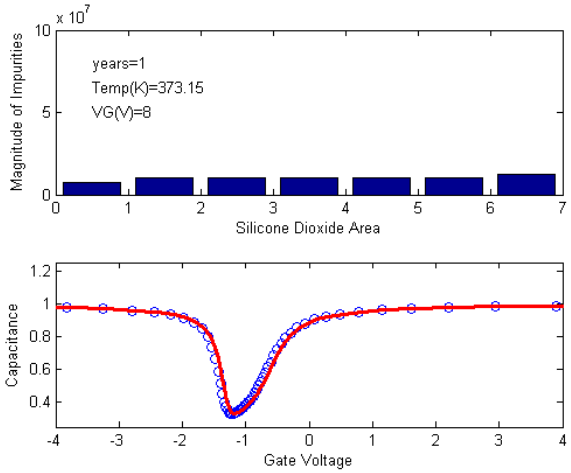

Figure 12: Migration of trap charges and capacitance variation at year 1 with 100°C and V_G =8V

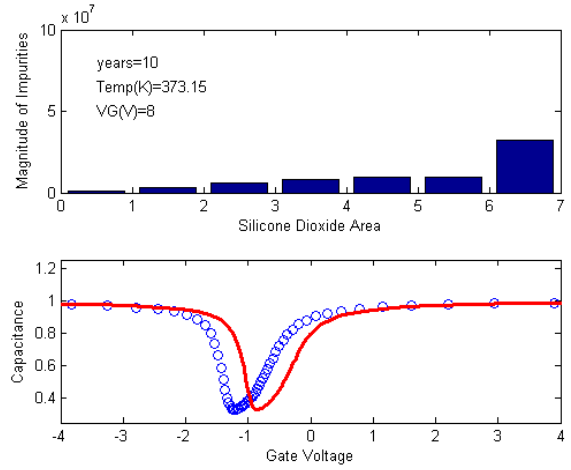

Figure 13: Migration of trap charges and capacitance variation at year 10 with 100°C and V_G =8V

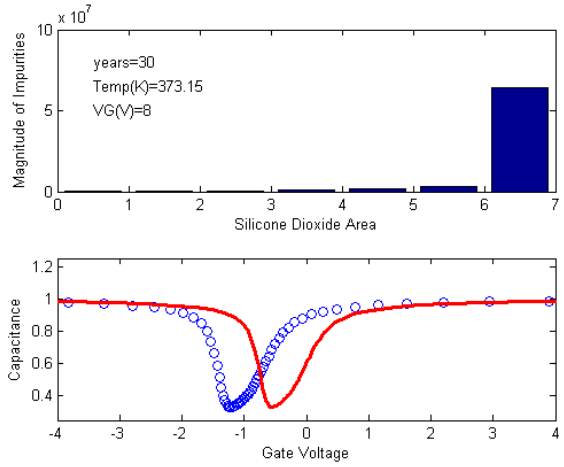

Figure 14: Migration of trap charges and capacitance variation at year 30 with 100°C and V_G =8V

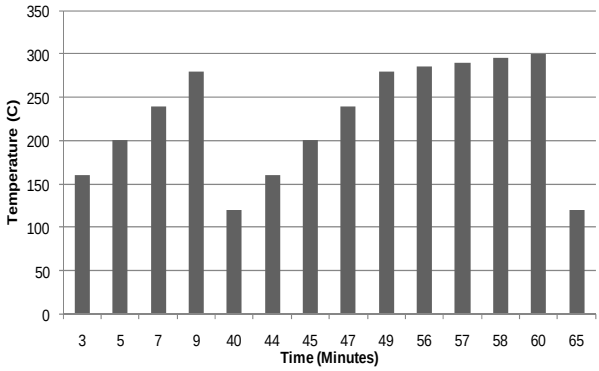

Figure 15: Temperature stress profile

Figure 16 shows the results of the shifting of the IGBT transistor capacitance as a function of the gate voltage. The normalized results show the shift in capacitance of the device before and after the device underwent the accelerated aging described in the previous section. As can be seen, the shifting of the device produces similar results to those obtained in the simulation. It should be noted that since MOSFETs and IGBTs have similar gate structure as describe earlier, the gate parasitic capacitance, that has been modeled and tested, would have similar results for both devices.

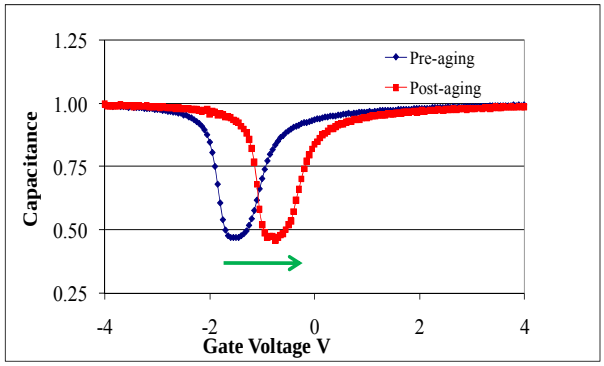

Figure 16: Capacitance shift of IGBT device before and after accelerated aging

7. CONCLUSION

Analytical and numerical relationships between the semiconductor physics-based behavior and stress factors through capacitance shifting was presented. This work successfully modeled the capacitance and the subsequent changing due to device aging. The combination of the aging stress voltages and temperature produces shifting in the impurities of oxide that modifies the relationship of the gate capacitance value and the gate voltages, resulting in a good indicator of device aging. As mentioned previously,

future work will also include the trap charge generation phenomenon in the modeling and validation.

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NOMENCLATURE

L(T)	life under thermal conditions
A, B	experimental constant
C, D	experimental constant
E	activation energy
T	temperature in Kelvin
k	Boltzmann's constant $8.6171.10^{-5}$ eV /^{o}C
$Si0_2$	Silicon dioxide
dt	time step
f, g	generic functions
I	current
N_A	total number of acceptor atoms/cm^3
q	magnitude of the electron charge (1.6×10^{-19} coul)
V	Voltage
Φ_S	Potential in the silicon
Φ_{ox}	Potential in the $Si0_2$
AF	Acceleration Factor
Co	Capacitance Value @ V_G=0
V_G	Gate Voltage

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